IN THE CLAIMS

1. (Original) A method of fabricating a multi-layer circuit board, the method comprising:

creating a first layer arrangement comprising a plurality of high-speed differential trace layers and a plurality of reference plane layers stacked in an interleaved fashion, each high-speed differential trace layer separated from each adjacent reference plane layer by a layer of a first dielectric material;

creating a second layer arrangement comprising at least two patterned power plane layers, each having a thickness at least equivalent to the thickness of three-ounces-per-square-foot copper, stacked between layers of a second dielectric material having better void-filling capability, during lamination under similar conditions, than the first dielectric material;

laminating the first and second layer arrangements together such that the first and second layer arrangements interface across a reference plane layer; and

forming a large plurality of plated thru-holes distributed throughout the circuit board, the plated thru-holes electrically connecting the reference plane layers, while leaving the power plane layers electrically isolated from each other and from the reference plane layers, within the circuit board.

2. (Original) The method of claim 1, further comprising:

creating a third layer arrangement comprising a plurality of high-speed differential trace layers and a plurality of reference plane layers stacked in an interleaved fashion, each high-speed differential trace layer separated from each adjacent reference plane layer by a layer of the first dielectric material;

stacking the first, second, and third layer arrangements in that order; and

laminating the stacked layer arrangements together such that the second and third layer arrangements interface across a reference plane layer.

3. (Original) The method of claim 2, wherein after laminating, the second layer arrangement is substantially at the middle of the multi-layer circuit board.

4. (Original) The method of claim 2, wherein the at least two patterned power plane layers comprise four power plane layers, electrically isolated from each other and from the reference plane layers, within the circuit board.

5. (Original) The method of claim 4, further comprising forming a second plurality of plated thru-holes in the circuit board, the second plurality of plated thru-holes respectively connecting the four power plane layers to first power return, first power supply, second power supply, and second power return connector areas on the board surface.

6. (Original) The method of claim 4, wherein the step of creating a second layer arrangement comprises stacking the power plane layers with at least one low-speed trace layer and at least one reference plane layer separating that low-speed trace layer from the power plane layers, that low-speed trace layer and reference plane each stacked between layers of the second dielectric material.

7. (Original) The method of claim 1, wherein the first dielectric material comprises an allylated polyphenylene ether and the second dielectric material comprises an FR-4 resin.

8. (Original) The method of claim 1, wherein the first dielectric material has a lower dielectric loss than the second dielectric material at high-speed signaling frequencies.

9. (Original) The method of claim 8, wherein the first and second dielectric materials each comprise, prior to assembly, sheets of woven glass fiber impregnated with a filler, the second dielectric material having a higher percent-filler content than the first dielectric material.

10. (Original) The method of claim 9, wherein two sheets of the first dielectric material separate each high-speed differential trace layer from each adjacent reference plane layer.

11. (Original) The method of claim 1, wherein the high-speed differential trace layers each comprise a board region within a larger panel region, the panel region

comprising a spaced-apart pattern of relatively small flow-impeding features near its periphery.

12. (Original) The method of claim 11, wherein the power plane layers comprise approximately the same board and panel regions as the high-speed differential trace layers, the panel region of each power plane layer comprising a substantially solid peripheral plane region having a relatively few patterned channels leading from the board region toward the edges of the panel.

13. - 24 (Canceled)